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Bifacial solar cell with SnS absorber by vapor transport deposition

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The SnS absorber layer in solar cell devices was produced by vapor transport deposition (VTD), which is a low-cost manufacturing method for solar modules. The performance of solar cells consisting of Si/Mo/SnS/ZnO/indium tin oxide (ITO) was limited by the SnS layer's surface texture and field-dependent carrier collection. For improved performance, a fluorine doped tin oxide (FTO) substrate was used in place of the Mo to smooth the topography of the VTD SnS and to make bifacial solar cells, which are potentially useful for multijunction applications. A bifacial SnS solar cell consisting of glass/FTO/SnS/CdS/ZnO/ITO demonstrated front- and back-side power conversion efficiencies of 1.2% and 0.2%, respectively. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4898092]

Vapor transport deposition (VTD) is a proven low-cost manufacturing method for commercial CdTe-based solar modules.[1,2] Strategies to further decrease the total cost of photovoltaic-generated energy for the consumer include (1) decreasing production costs and (2) improving the power conversion efficiency (η) of the solar modules without significantly adding costs. For providing a substantial portion of society's energy needs, SnS is a potentially low-cost material for mass production because it can be produced by VTD and its constituents are non-toxic and earth abundant. Most recently, a 4.4% SnS-based solar was demonstrated.[3] If high performance SnS-based solar cells can be fabricated using VTD, commercial adoption can also leverage existing manufacturing equipment. SnS, therefore, has high prospects for use in solar cells.

Additionally, because SnS has a bandgap of 1.0 eV, it can serve either as a single-junction solar cell or as the bottom cell of a dual junction solar cell consisting of CdTe- and SnS-based devices. SnS can capture unused light that is transmitted through the CdTe layer. Such a multijunction device has a theoretical η of about 40%,[4] which addresses the second strategy for reducing the overall cost of photovoltaic energy. In the future, flat-panel multijunction solar modules could be manufactured based on VTD and deployed at low cost, eliminating the need for concentrators. As the best performing SnS solar cells reported thus far have been produced by spray pyrolysis,[5] sputtering,[6] and chemical vapor deposition,[7] our work on SnS solar cells produced by the potentially lower cost method of VTD strengthens the impact that SnS can have on commercial photovoltaic energy generation.

Whereas previous reports on SnS solar cells all involve a metal back contact, this study explores the use of a transparent conducting oxide substrate to make bifacial solar cells with improved performance. In practice, bifacial solar cells are advantageous because they can produce more power than a single-sided cell by capturing the light reflected from the environment (albedo) onto the rear surface.[8] Bifacial cells are also useful for making 4-terminal dual junction devices,[9] as unused light from the top cell can be transmitted to the bottom cell. In addition to these advantages, we demonstrate below that an fluorine doped tin oxide (FTO) substrate can reduce the surface texture of SnS deposited by VTD.

SnS solar cells can be produced using the standard copper indium gallium diselenide (CIGS) device architecture, by replacing the CIGS absorber layer with SnS. Specifically, SnS can be deposited onto a Mo-coated glass substrate, followed by chemical bath deposited CdS at 65 °C and sputter-deposited ZnO-Al:ZnO (AZO) at room temperature.[10] The CdS layer is usually referred to as the buffer layer, whereas the ZnO-AZO is referred to as the transparent conducting oxide (TCO) bilayer. As the CIGS architecture has been optimized for CIGS, ultimately it may not be the best design choice for SnS because of the different interfaces present. We therefore explored various back contacts, buffer layers and TCO bilayers for SnS-based solar cells.

The SnS layers in this study were all produced by the VTD method described from our previous work[11] with minor modifications to increase the deposition rate. Specifically, SnS powder was heated in a multi-zone horizontal tube furnace to 500 °C for 1.5 h with flowing N_2 at 5 sccm and up to 100 mTorr. The substrate was placed 10 in. downstream at 365 °C. All of the devices had an area of 0.01 cm^2 as defined by the patterned TCO and were tested under AM 1.5G illumination using an Oriel Sol3A Class AAA Solar Simulator and a Keithley 2420 sourcemeter.

Fig. 1 shows the cross sectional scanning electron microscope (SEM) image of a device stack of Si/Mo/SnS/ZnO/indium tin oxide (ITO), with layer thicknesses of about 0.5 μm, 1 μm, 30 nm, and 100 nm for the Mo, SnS, ZnO, and ITO layers, respectively. There is considerable surface texture due to the large, irregularly shaped crystalline grains of SnS. Despite the surface texture and lack of a buffer layer, this device produced an open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}) and η of 240 mV, 9.0 mA/cm^2, and 0.6%, respectively, under AM 1.5G illumination (see Fig. 2).

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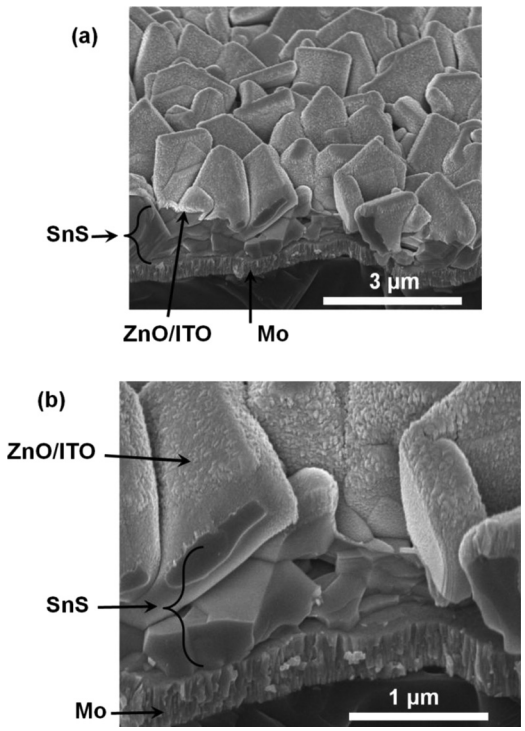

FIG. 1. 45°-tilted SEM cross-sectional images of (a) Si/Mo/SnS/ZnO/ITO and (b) the same device under higher magnification.

It is clear from Fig. 1 that the ZnO-ITO bilayer conformally covers the SnS top surface. While the seemingly large SnS crystalline grains may be beneficial for improving charge carrier collection, the accompanying surface texture leads to high series resistance (R_s) in the TCO. As resistance is directly related to the length that the free electrons have to travel in the transparent conductor, the unwieldy path over the SnS surface could be detrimental to solar cell performance. The normalized R_s estimated from the slope of the illuminated current-voltage (JV) curve (solid line of Fig. 2) at open-circuit is 15 Ω cm^2, which is detrimental to the fill factor (FF) and η. The R_s calculated at V_{oc} should be considered as a rough estimate, however, since virtual shunting (to be explained more below) and other non-idealities such as other extra series-connected diodes (e.g., Schottky back contact (SBC)) can also affect the slope at V_{oc}. Moreover, the diode conductance increases with voltage beyond open-circuit, indicating that the

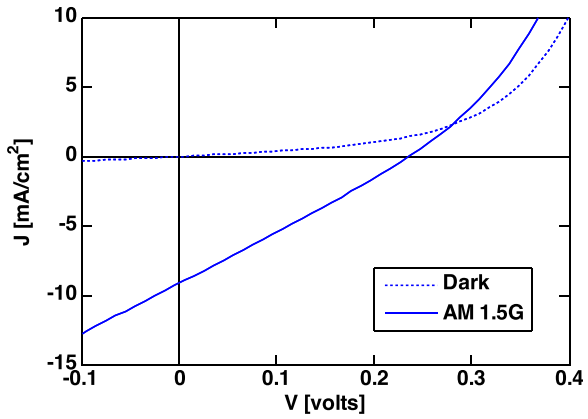

FIG. 2. Si/Mo/SnS/ZnO/ITO solar cell JV plot. Both dark (broken line) and AM 1.5G illuminated curves (solid line) are plotted.

actual R_s is less than 15 Ω-cm^2. In separate work, we are developing a better method for quantifying R_s.

In addition to increasing R_s, the rough film also increases the area of the metallurgical junction of the p-n junction. This can be seen from the ideal diode equation to increase the magnitude of dark forward current at a given applied bias.[12] Assuming that the photo-generated current and the dark current add to produce the illuminated JV behavior, an increase in junction area leads to a decrease in V_{oc}. Therefore, it is preferable to reduce the surface texture not only to decrease R_s but also to decrease the dark forward current.

Other issues to be addressed to increase performance include charge carrier collection. The J_{sc} for our device is less than that of the world record SnS devices.[3] This deficit can be accounted for by poor absorption, poor charge carrier collection or a combination of both. Calculations using diffuse reflectance and transmittance spectra suggest that poor absorption in the SnS layer contributes to significant optical losses throughout the device (totaling about 20 mA/cm^2), but optical losses are not the only cause of the low J_{sc}.[10] The maximum J_{sc} density assuming perfect quantum efficiency was calculated to be 28 mA/cm^2. Since this value is much larger than the actual J_{sc} we measured, poor charge carrier collection is a higher priority to address. Optical losses throughout the device can be addressed after the charge collection efficiency within the SnS layer is adequate.

The slopes at zero bias for the dark and illuminated JV behavior in Fig. 2 indicate poor carrier collection in the device. Since the two slopes are significantly different, the slope for the illuminated curve must be due mainly to an issue not involving shunting. The slope of the illuminated curve at J_{sc} can be attributed to drift-assisted charge carrier collection, which is sometimes referred to as a virtual shunt. As the bias across the p-n junction goes from positive to negative, the depletion volume and its associated electric field magnitude in the SnS layer increases. With the stronger electric field occupying more volume in the SnS, more charge carriers can be collected by drift. Virtual shunting is thus a symptom of poor carrier collection by diffusion in the absence of an electric field. The low FF arising from virtual shunting and high R_s are major impediments to higher performing devices.

To address these issues, an FTO substrate (TEC 15 FTO) was employed. As shown in Figs. 3 and 4, the surface texture of the SnS deposited on FTO appears less pronounced compared to that of Fig. 1. In both cases, the SnS layer was deposited under the same VTD conditions. Solar cells consisting of the stack glass/FTO/SnS/ZnO/ITO were tested and achieved V_{oc}, J_{sc}, FF, and η of 300 mV, 2 mA/cm^2, 0.28, and 0.17%, respectively. The reduction in surface texture may have increased the V_{oc} by decreasing the metallurgical junction area of the SnS-ZnO p-n heterojunction, which decreases the dark forward current as explained above. Although the V_{oc} and FF increased slightly, the decrease in J_{sc} resulted in no improvement in overall η. The J_{sc} may be improved by mitigating sputter damage as discussed next.

In order to further improve J_{sc}, we sought to protect the SnS surface from energetic particles in the sputtering process

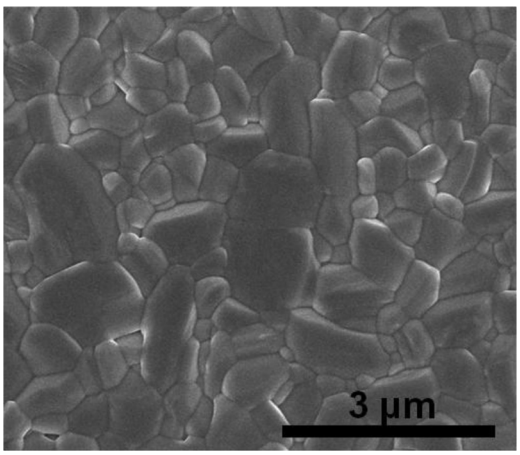

FIG. 3. Plan view SEM image of SnS grown by VTD on glass/FTO substrate.

by depositing buffer layers by CBD and atomic layer deposition (ALD). First, we deposited ZnO and TiO_2 by ALD.[10] Our devices exhibited no rectification behavior when buffer layers by ALD were used. The precursors and temperatures used in the ALD processes may have damaged the SnS layers we fabricated by VTD. Zn(O,S) buffer layers formed by CBD achieved rectification behavior, but the V_{oc} and J_{sc} were both low. Tuning the O-to-S ratio may have helped to optimize the band alignment at the interface,[7] but such capabilities were not available to us. The most functional buffer layer for our solar cells was found to be CdS by CBD. The device architecture glass/FTO/SnS/CdS/ZnO/ITO is thus discussed here in more detail.

Shown in Fig. 5 is the JV data for the glass/FTO/SnS/CdS/ZnO/ITO device. The curve labeled "frontside" refers to AM 1.5G illumination from the ITO side. Compared to Fig. 2, although the V_{oc} is lower at 200 mV, the J_{sc} improved to 15 mA/cm^2. The FF increased significantly to 0.40, reflecting less virtual shunting than in the previous architectures. Overall, this architecture resulted in our highest performing device at $\eta = 1.2\%$. Since ITO and FTO are both transparent conductors, this solar cell can be illuminated from both sides and operate as a bifacial solar cell. We measured the JV characteristics of the same device under AM 1.5G illumination through the underside (glass/FTO). As shown in Fig. 5,

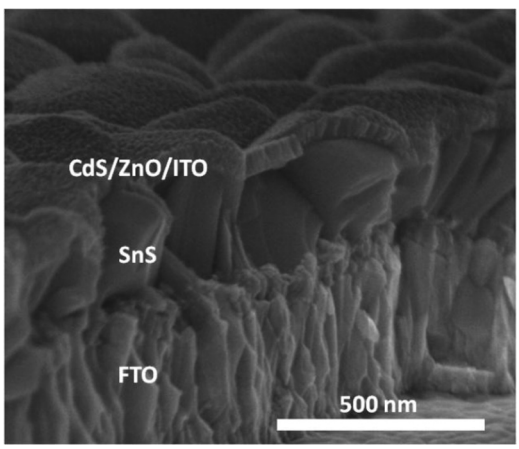

FIG. 4. SEM cross-sectional image of glass/FTO/SnS/CdS/ZnO/ITO bifacial solar cell.

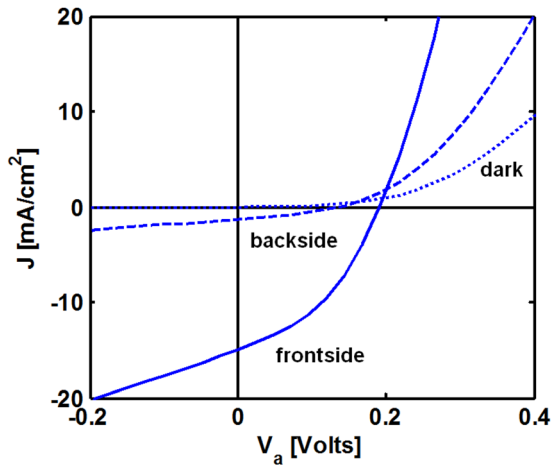

FIG. 5. JV data for the solar cell device made of glass/FTO/SnS/CdS/ZnO/ITO. Plotted are curves for the solar cell in the dark (dotted line), under frontside AM 1.5G illumination (solid line), and under backside AM 1.5G illumination (dashed line).

the V_{oc}, J_{sc}, FF, and η in this configuration are 140 mV, 1.3 mA/cm^2, 0.34, and 0.2%, respectively.

Based on the lower J_{sc} during backside illumination, the diffusion length of minority carrier electrons in the p-type SnS appears to be less than the thickness of the device (~400 nm) because the photogenerated minority carrier electrons at the back side do not get collected adequately at the SnS/CdS interface to contribute significantly to J_{sc}. Both the low backside J_{sc} and the virtual shunt indicate that the J_{sc} can increase by improving charge carrier collection. Two options for improving charge carrier collection include: (1) improving the minority carrier diffusion length in the bulk SnS by increasing minority carrier mobility, minority carrier lifetime or both and (2) using a thinner SnS layer to reduce charge carrier collection distance necessary. For the latter, light trapping techniques may be necessary to maintain adequate light absorption. Nanostructuring the p-n junction can also reduce the charge carrier collection distance required.[13]

Photo-generation and collection of minority carrier electrons at the SBC have previously been attributed as a cause of the cross-over effect for CdTe-based solar cell devices of the architecture Au/CdTe/CdS/TCO.[14] At an appreciable applied forward bias, the illuminated curve begins to overtake (cross-over) the dark curve in current. In the presence of the SBC, the dark and illuminated JV curves would not follow the simple principle of superposition. As apparent from the JV curves of Fig. 5, our SnS-based solar cells also exhibit the cross-over effect. However, the data for our SnS-based solar cells do not support the existence of a SBC at the FTO/SnS interface.

The negative J_{sc} during backside illumination indicates the absence of a SBC. If a SBC was to be present, as depicted by the hypothetical band diagram in Fig. S2(a).[10] backside illumination would cause the photo-generated minority carrier electrons in the conduction band of SnS to drift to the back contact by the SBC's built-in electric field. Inversely, the holes in the valence band would drift away from the back contact into the SnS. The resulting J_{sc} would be positive, since it is in the direction of forward current as defined by the applied voltage across the p-n junction. The

negative J_{sc} we measured, therefore, indicates that the FTO/SnS interface is ohmic for holes.

Since the cross-over effect is more pronounced during front-side illumination (Fig. 5), a physical contributor to the enhanced forward current giving rise to the cross-over effect should exist at the front of the device. Besides the SBC discussed above, Fig. S2(b) illustrates another possible mechanism at the front that may enhance the forward current leading to the cross-over effect. Majority carrier electrons from the N-type side need to surmount the junction barrier to contribute to forward current. The free-carrier absorption process can provide energy for the electrons to surmount the barrier. Free-carrier absorption can occur when free electrons in the conduction band absorb infrared radiation. If the infrared photons have more energy than the barrier or potential spike impeding electron flow, the current can increase as a result. As the SnS/CdS interface is reported to have a considerable conduction band barrier,[15] this mechanism for the cross-over effect may be more significant than the SBC.

In summary, bifacial polycrystalline SnS solar cell devices were produced using VTD with η as high as 1.2%. VTD is a proven technique known for manufacturing CdTe solar cells at low cost, thereby offering routes for SnS to be a commercially viable solar cell material as an absorber. An FTO back contact was used to reduce surface texture of the SnS layer. The CdS buffer layer was next deposited by CBD to protect the SnS surface from sputter damage. Finally, ZnO/ITO was deposited by sputtering. This architecture produces power when illuminated from either side and thus demonstrates a bifacial SnS solar cell. Backside illumination indicates that the FTO/SnS interface is ohmic for holes.

Despite improvements in surface texture, R_s and FF, many other issues need to be addressed. We have identified several improvement pathways: increasing minority carrier diffusion length, thinning the SnS absorber layer, and using a buffer layer with better band alignment and benign deposition conditions. It would also be beneficial to further reduce the SnS surface texture with epitaxial SnS films, which we have shown to have smoother morphology as well as higher mobility.[11] Assuming that such epitaxially grown films contain fewer defects, the improvements in minority carrier lifetime and mobility would also increase the minority carrier diffusion length. With the plethora of routes available to improve SnS-based solar cells, there is potential for a significantly higher performing device to be engineered in the near future using low cost vapor transport deposition.

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